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Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
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| | 09/815,778 | KHANNA, SANDEEP | |
| | Examiner | Art Unit | |
| | Cynthia L Davis | 2665 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *7/15/2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-54* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-54* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Response to Arguments*

1. Applicant's arguments filed 7/15/2005 have been fully considered but they are not persuasive.

Regarding claims 1-49, Srinivasan discloses two memory blocks, and also discloses using incremental comparisons to choose the highest priority match out of a group of matches that match a search key word. This reads on the claim language of claims 1, 29, and 44.

Regarding claims 50-54, Srinivasan does contain all the elements of claim 50 that applicant claims are missing. See rejection of claim 50, below.

### *Claim Rejections - 35 USC § 102*

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 29-35, 37-40, and 44-49 are rejected under 35 U.S.C. 102(b) as being anticipated by Srinivasan.

Regarding claim 29, determining a first block priority number from a first plurality of priority numbers where each of the first plurality of priority numbers are associated with data stored in a first data classification block (DCB) that matches a search key; determining a second block priority number from a second plurality of priority numbers where each of the second plurality of priority numbers are associated with data stored in a second DCB that match the search key; and determining a most significant block priority number (MSBPN) from the first block priority number and the second block

priority number is disclosed in Srinivasan in column 2, lines 41-50 (disclosing a method for determining the highest priority match from a group of matches in a memory), and column 5, Lines 59-column 6, Line 15 (disclosing the use of incremental comparisons to search using multiple search words).

Regarding claim 30, further comprising generating a device index of data associated with the most significant priority number is disclosed in column 4, Lines 33-36 (the address of the most significant data is generated, this is equivalent to the index).

Regarding claim 31, determining a first block index associated with the first block priority number; and determining a second block index associated with the second block priority number is disclosed in column 4, lines 33-36 (the address of the most significant data is generated for all searches, this is equivalent to the index).

Regarding claim 32, determining which of the first and second data classification blocks originates the MSBPN; and transmitting enable signals to the first and second DCBS that indicate whether a DCB originates the MSBPN is disclosed in column 2, lines 41-50 (the match signals are sent from each block in the memory to indicate where the matches occurred).

Regarding claim 33, generating a first match flag signal that indicates whether the MSBPN originates from the first DCB; and generating a second match flag signal that indicates whether the MSBPN originates from the second DCB is disclosed in column 2, Lines 41-50 (the match signals are sent from each block in the memory to indicate where the matches occurred).

Regarding claim 34, storing the first block index in a first storage element having a first address; and storing the second block index in a second storage element having a second address is disclosed in column 4, lines 33-36 (the addresses of all of the matches are made available to the priority encoder so that it may select the highest priority one).

Regarding claim 35, encoding a match flag signal received into a most significant block identifier, decoding the most significant block identifier into an address of a storage element that stores a block index output from a data classification block corresponding to the most significant block index; outputting a most significant block index in response to asserting the address, and generating a device index from the most significant block identifier and the most significant block index is disclosed in column 2, Lines 46-47 (match flag signal) and column 4, Lines 33-36 (the addresses/device indices of all of the matches are made available to the priority encoder so that it may select the highest priority one).

Regarding claim 37, the first and second block priority numbers comprise a plurality of sub-block priority numbers (SBPN) is disclosed in column 2, line 48 (the various blocks could also be viewed as sub-blocks; there are a plurality of blocks each with a priority number).

Regarding claim 38, determining which of the first and second DCBS originates the MSBPN comprises: determining a first most significant sub-block priority number (MSSBPN) from a first SBPN from the first DCB and a first SBPN from the second DCB and outputting first compare logic circuit control signals that indicate which DCB

originates the first MSSBPN, and determining a second MSSBPN from a second SBPN from the first DCB and a second SBPN from the second DCB, where each of the second SBPN from the first and second DCBS is assigned a least significant sub-block priority number (LSSBPN) if the first MSSBPN did not originate from its DCB, and outputting second compare logic circuit control signals that indicate which DCB originates the first and second MSSBPNS is disclosed in column 2, Lines 41-50 (match or non-match signals, equivalent to most or least significance, are generated by all blocks).

Regarding claim 39, determining which of the first and second DCBS originates the MSBPN further comprises determining a third MSSBPN from a third SBPN from the first DCB and a third SBPN from the second DCB, where each of the third SBPNS from the first and second DCBS is assigned the LSBPN if the first and second MSSBPNS did not originate from its DCB, and outputting third compare logic circuit control signals that indicate which DCB originate the first, second, and third MSSBPN, where the DCB that originates the third MSSBPN is the DCB that originates the MSBPN is disclosed in column 2, Lines 41-50 (match or non-match signals, equivalent to most or least significance, are generated by all of the plurality of blocks).

Regarding claim 40, transmitting the third compare logic control signals as enable signals to the first and second DCBS that indicate whether the MSBPN originates from it is disclosed in column 2, Lines 41-50 (match or non-match signals, equivalent to enable or non-enable signals, are generated by all of the plurality of blocks).

Regarding claim 44, a digital signal processor comprising: means for determining a first block priority number (BPN) associated with a first data stored in a first data classification block (DCB) that matches a search key; means for determining a second BPN associated with a second data stored in a second DCB that matches the search key; and means for determining a most significant block priority number (MSBPN) from the first BPN and the second BPN is disclosed in Srinivasan, column 2, lines 41-50.

Regarding claim 45, the means for determining the first block priority number determines a first block index associated with the first data, and the means for determining the second priority number determines a second block index associated with the second data is disclosed in column 4, lines 33-36 (the addresses for the matches, which are related closely to the indices, are determined for all matches).

Regarding claim 46, the means for determining the MSBPN comprises: means for determining the MSBPN from the first BPN and the second BPN; and means for determining enable signals that indicate which DCBS originate the MSéPN is disclosed in column 2, lines 46-47 (the match, or enable, signals indicate a match)

Regarding claim 47, the means for determining the first BPN determines a first match flag signal that indicates whether the MSBPN originates from the first DCB and the means for determining the second BPN determines a second match flag signal that indicates whether the MSBPN originates from the DCB is disclosed in column 2, lines 46-47 (the match signals indicate whether the MSBPNS originate from the DCBs).

Regarding claim 48, the means for determining the MSBPN further comprises a means for determining a device index from the first and second block indices and the

first and second match flag signals is disclosed in column 4, Lines 33-36 (the addresses for the matches, which are related closely to the indices, are determined for all matches).

Regarding claim 49, the means for determining the MSBPN from the first BPN and the second BPN includes: means for determining a first most significant sub-block priority number (MSSBPN) from a first sub-block priority number (SBPN) from the first DCB and a SBPN from the second DCB, and that outputs first compare logic circuit control signals that indicate which DCB originates the first MSSBPN; and means for determining a second MSSBPN from a second SBPN from the first DCB and a second SBPN from the second DCB, and that outputs second compare logic circuit control signals that indicate which DCB originates the first and second MSSBPNS, where each of the second SBPN from the first and second DCBS is assigned a least significant sub block priority number (LSSBPN) if the first MSSBPN did not originate from its DCB is disclosed in column 2, lines 41-47 (each block/subblock has a comparator; the non-matching blocks generate match signals, equivalent to MSSBPNS, and no-match signals, equivalent to a LSBPN).

***Claim Rejections - 35 USC § 103***

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

3. Claims 1-26, 28, and 50-54 are rejected under 35 U.S.C. 103(a) as being unpatentable over Srinivasan in view of Williams.

Regarding claim 1, a first data classification block (DCB) that outputs a first block priority number (BPN) associated with a first data stored in the first DCB that matches a search key; a second DCB that outputs a second BPN associated with a second data stored in the second DCB that matches the search key; and a device index processor that determines a most significant block priority number (MSBPN) from the first BPN and the second BPN is disclosed in Srinivasan, column 2, Lines 41-50 (disclosing a memory with a plurality of blocks, all of which are searched for matches, and then the highest priority match is chosen from the matches). A digital signal processor is missing from Srinivasan. However, Williams discloses in column 4, Lines 45-47, a CAM, such as is disclosed in Srinivasan, that may be implemented in a DSP. It would have been obvious to one skilled in the art to implement the CAM of Srinivasan in a DSP. The motivation would be to use a commonly available type of hardware to implement the CAM.

Regarding claim 2, the device index processor outputs a device index for data associated with the MSBPN is disclosed in Srinivasan, column 4, lines 33-36 (the address of the highest priority word is outputted; the address is equivalent to the device index).

Regarding claim 3, the first DCB outputs a first block index associated with the first data, and the second DCB outputs a second block index associated with the second data is disclosed in column 4, lines 33-36 (the addresses of all of the matches are made available to the priority encoder so that it may select the highest priority one).

Regarding claim 4, the device index processor comprises: a compare logic that determines the MSBPN from the first BPN and the second BPN; and an inhibit signal generator that outputs enable signals that indicate which DCBS originate the MSBPN is disclosed in Srinivasan, column 2, Lines 46-47.

Regarding claim 5, the inhibit signal generator comprises a plurality of comparator circuits is disclosed in Srinivasan, column 2, Lines 46-47.

Regarding claim 6, the first DCB outputs a first match flag signal that indicates whether the MSBPN originates from the first DCB, and the second DCB outputs a second match flag signal that indicates whether the MSBPN originates from the second DCB is disclosed in column 2, Lines 46-47.

Regarding claim 7, a priority logic that compares priority numbers in the priority memory associated with data in the data table that match the search key and provides an indication of a most significant priority number as a BPN for the DCB on a match line segment; a row enable logic that propagates the indication of the BPN on the match line segment in response to receiving the enable signal; a match flag generator that outputs a match flag signal that indicates whether the BPN for the DCB is the MSBPN in response to the row enable logic propagating the indication, and an encoder that generates an index relative to the DCB associated with the indication propagated by the row enable logic are disclosed in Srinivasan, column 2, Lines 41-50 (match lines and comparators), figure 2, element 30 (the priority encoder) and column 4, lines 33-36 (the address of the highest priority data, which is equivalent to the index). A data table that stores data, and a priority memory that stores a plurality of priority numbers, each

priority number associated with a corresponding data in the data table and indicating a priority of the corresponding data relative to other data in the data table is missing from Srinivasan. However, Williams discloses in column 7, Lines 43-48, a data table that includes a priority field. It would have been obvious to one skilled in the art at the time of the invention to have priority numbers associated with data in a table. The motivation would be to indicate the relative priority of data in the table for routing purposes.

Regarding claim 8, the row enable logic comprises a plurality of circuits that perform an AND function is not specifically disclosed in Srinivasan. However, the AND function is well known in the ad. It would have been obvious to one skilled in the art at the time of the invention to use an AND function. The motivation would be to use a well known function for which hardware is readily available.

Regarding claim 9, the match flag generator comprises a circuit that performs an OR function is not specifically disclosed in Srinivasan. However, the OR function is well known in the art. It would have been obvious to one skilled in the ad at the time of the invention to use an OR function. The motivation would be to use a well known function for which hardware is readily available.

Regarding claim 10, the device index processor further comprises an address generator that determines a device index from the first and second block indices and the first and second match flag signals is disclosed in column 4, Lines 33-36 (the address of the highest priority match is generated from the match signals). Regarding claim 11, the address generator comprises a priority encoder that outputs a block identifier that identifies a DCB that originates the MSBPN, and when both the first and

second DCBS originate the MSBPN, the priority encoder outputs a block identifier corresponding to a DCB that has a higher priority is disclosed in column 4 ,lines 33-36 of Srinivasan.

Regarding claim 12, the address generator further comprises an index storage unit that includes: a first storage element, having a first address, that stores the first block index; and a second storage element, having a second address that stores the second block index is disclosed in column 4, Lines 33-36 (the addresses of all of the matches are made available to the priority encoder so that it may select the highest priority one).

Regarding claim 13, the address generator further comprises a decoder that decodes the block identifier output from the priority encoder into an address of a storage element that stores a block index output from a data classification block corresponding to the block identifier is disclosed in column 4, Lines 33-36 (the addresses of all of the matches are made available to the priority encoder so that it may select the highest priority one).

Regarding claim 14, the address generator further comprises a multiplexer that receives the first and second block indices is disclosed in column 4, lines 33-36 (the priority encoder acts as a multiplexer that receives both block addresses).

Regarding claim 15, the address generator further comprises a decoder that decodes the block identifier output from the priority encoder and selects one of the first and second block indices to be output from the multiplexer in response to the block identifier is disclosed in column 4, Lines 38-42.

Regarding claim 16, further comprising an index generator that outputs the device index for data associated with the MSBPN, the index generator designating the block identifier output from the priority encoder as the most significant bits of the device index and a block index output from the multiplexer as the least significant bits of the device index is disclosed in column 4, Lines 33-36 (the address for the most significant data is output).

Regarding claim 17, the compare logic includes: a first compare logic circuit that determines a first most significant sub-block priority number (MSSBPN) from a first sub-block priority number (SBPN) from the first DCB and a SBPN from the second DCB, and that outputs first compare logic circuit control signals that indicate which DCB originates the first MSSBPN is disclosed in column 2, Lines 41-47 (a comparison is done in the memory with a plurality of blocks, any block of which may be viewed as a subblock, and a match signal generated). A second compare logic circuit that determines a second MSSBPN from a second SBPN from the first DCB and a second SBPN from the second DCB, and that outputs second compare logic circuit control signals that indicate which DCB originates the first and second MSSBPNS, where each of the second SBPN from the first and second DCBS is assigned a least significant sub-block priority number (LSBPN) if the first MSSBPN did not originate from its DCB is disclosed in column 2, Lines 41-47 (each block/subblock has a comparator, the non-matching blocks generate no-match signals, which is equivalent to a LSBPN).

Regarding claim 18, the first compare logic circuit comprises: a first stage comparator for the first compare logic circuit that compares the first SBPNS from the

first and second DCBS to determine the first MSSBPN, a first second stage comparator for the first compare logic circuit that compares the first MSSBPN with the first SBPN from the first DCB and that generates a first control signal that indicates whether the first MSSBPN originates from the first DCB; and a second second stage comparator for the first compare logic circuit that compares the first MSSBPN with the first SBPN from the second DCB and that generates a second control signal that indicates whether the first MSSBPN originates from the second DCB is not specifically disclosed in Srinivasan. However, in column 2, lines 41-47, it is disclosed that the system uses comparators to find matches in a plurality of memory blocks, and generates match (control) signals, which is exactly what the claimed invention does. It would have been obvious to one skilled in the art at the time of the invention to use the described series of comparators to implement the method of Srinivasan. The motivation would be to have a hardware implementation for the method.

Regarding claim 19, the first and second stage comparators each comprises a plurality of circuits that perform an XNOR function with outputs coupled to a circuit that performs an AND function is not specifically disclosed in Srinivasan. However, the XNOR and AND functions are well known in the art. It would have been obvious to one skilled in the ad at the time of the invention to use XNOR and AND functions. The motivation would be to use a well known functions for which hardware is readily available.

Regarding claim 20, the second compare logic circuit comprises: a compare enable circuit that assigns a LSSBPN to the second SBPN from the first DCB upon

receiving a first control signal that indicates that the first MSSBPN did not originate from the first DCB, and that assigns a LSSBPN to the second SBPN from the second DCB upon receiving a second control signal that indicates that the first MSSBPN did not originate from the second DCB; a first stage comparator for the second compare logic circuit that compares the second SBPNS from the first and second DCBS to determine the second MSSBPN, a first second stage comparator for the second compare logic circuit that compares the second MSSBPN with the second SBPN from the first DCB and that generates a first output that indicates whether there is a match', and a second second stage comparator for the second compare logic circuit that compares the second MSSBPN with the second SBPN from the second DCB and that generates a second output that indicates whether there is a match is not specifically disclosed in Srinivasan. However, in column 2, Lines 41-47, it is disclosed that the system uses comparators to find matches in a plurality of memory blocks, and generates match (control) signals, which is exactly what the claimed invention does. It would have been obvious to one skilled in the art at the time of the invention to use the described series of comparators to implement the method of Srinivasan. The motivation would be to have a hardware implementation for the method.

Regarding claim 21, the second compare logic further comprises: a first control signal processor that receives the first control signal and the first output and that generates a third control signal that indicates whether the first and second MSSBPNS originate from the first DCB; and a second control signal processor that receives the second control signal and the second output and that generates a fourth control signal

that indicates whether the first and second MSSBPNS originate from the second DCB match is not specifically disclosed in Srinivasan. However, in column 2, Lines 41-47, it is disclosed that the system uses comparators to find matches in a plurality of memory blocks, generates match (control) signals, and determines which matching data is the highest priority, which is exactly what the claimed invention does. It would have been obvious to one skilled in the art at the time of the invention to use the described series of comparators to implement the method of Srinivasan. The motivation would be to have a hardware implementation for the method.

Regarding claim 22, each of the first and second control signal processors comprises a circuit that performs an OR function is not specifically disclosed in Srinivasan. However, the OR function is well known in the art. It would have been obvious to one skilled in the art at the time of the invention to use an OR function. The motivation would be to use a well known function for which hardware is readily available.

Regarding claim 23, the compare logic further comprises a third compare logic circuit that determines a third MSSBPN from a third SBPN from the first DCB and a third SBPN from the second DCB, and that outputs third compare logic circuit control signals that indicate which DCB originates the first, second, and third MSSBPNS, where each of the third SBPNS from the first and second DCBS is assigned the LSBPN if the first and second MSSBPNS did not originate from its DCB However, in column 2, Lines 41-47, it is disclosed that the system uses comparators to find matches in a plurality of memory blocks, generates match (control) signals, and determines which matching data

is the highest priority, which is exactly what the claimed invention does. It would have been obvious to one skilled in the art at the time of the invention to use the described series of comparators to implement the method of Srinivasan. The motivation would be to have a hardware implementation for the method.

Regarding claim 24, the third compare logic circuit control signals are transmitted to the first and second DCBS as enable signals that indicate whether a DCB originates the MSBPN is disclosed in column 2, lines 33-36 (the match signals are enable signals indicating a match).

Regarding claim 25, the first compare logic circuit comprises a first priority index table and the second compare logic circuit comprises a second priority index table is missing from Srinivasan. However, Williams discloses in column 7, Lines 43-48, a data table that includes a priority field. It would have been obvious to one skilled in the art at the time of the invention to have priority numbers associated with data in a table. The motivation would be to indicate the relative priority of data in the table for routing purposes.

Regarding claim 26, the DCB stores Internet Protocol addresses and the first and second BPNS comprise prefix mask data for the Internet Protocol addresses is missing from Srinivasan. However, Williams discloses in column 6, line 45, and column 7, Lines 43-48, a connection table. It would have been obvious to one skilled in the art at the time of the invention to use IP addresses and prefix mask data to describe the connections. The motivation would be to use an inherent quality of the connections to describe them.

Regarding claim 28, the DCB includes a content addressable memory (CAM) array is disclosed in column 2, Line 41 of Srinivasan.

Regarding claim 50, a data table that stores uniquely addressable data entries is disclosed in column 2, Line 41 (the CAM cells), a row enable logic circuit is disclosed in column 2, Lines 42-45 (a comparator that decides if there is a match, i.e., if the row should be enabled; a priority index table is disclosed in column 2, Line 48 (each entry has an associated priority, if it didn't there would be no way to select the highest priority match); a match flag signal generator coupled to the row enable logic circuit is disclosed in column 2, lines 46-47, an encoder coupled to the row enable encoder circuit is disclosed in column 4, lines 33-34, and a device index processor coupled to the plurality of priority index tables, match flag signal generators, and row enable encoder circuits to determine the index for at least one of the data entries that matches a search key is disclosed in column 4, Lines 36-42 (the address decoder). A digital signal processor is missing from Srinivasan. This is disclosed in Williams, column 4, Lines 46-47 (a DSP). It would have been obvious to one skilled in the art at the time of the invention to use the system of Srinivasan in the priority-based routing DSP of Williams. The motivation would be to process priority data in a network (see Srinivasan, column 2, line 17).

Regarding claim 51, each priority index table comprises: memory that stores priority numbers for each corresponding data entry; and compare logic that determine a most significant priority number for the data classification block is disclosed in column 2, lines 47-50 (each block has a priority number, so as to be able to select the most significant priority number, the priority encoder acts as the compare logic).

Regarding claim 52, each row enable logic circuit comprises circuitry that processes signals on internal address lines from the priority index table and an enable signal from the device index processor is disclosed in column 2, Lines 42-50 (the row enable logic gets signals from the priority table so it can send the priority of the match, if there is one).

Regarding claim 53, each match flag signal generator comprises circuitry that processes signals on internal address lines from the row enable logic circuit is disclosed in column 2, lines 46-47.

Regarding claim 54, the device index processor comprises: a compare logic; an inhibit signal generator coupled to the compare logic, and a device index generator coupled to the plurality of data classification blocks is not specifically disclosed in Srinivasan. However, Srinivasan discloses in column 4, Lines 36-42, an element (the address decoder) that does what the device described here does. It would have been obvious to one skilled in the art at the time of the invention to construct the address decoder in the manner described above. The motivation would be to determine the address of the highest priority data.

4. Claim 27 is rejected under 35 U.S.C. 1'03(a) as being unpatentable over Srinivasan in view of Williams in further view of Rogers.

Regarding claim 27,the DCB stores policy statement and the first and second BPNS indicate the relative priority of the policy statements is missing from Srinivasan. However, storing policy statements in a memory and interpreting them based on

network conditions (for which one would need to know their relative priority) is disclosed in Rogers, column 5, lines 37-42 and 52-54. It would have been obvious to one skilled in the art at the time of the invention to store the policy statements and their relative priority. The motivation would be to have the policy statements available for routing purposes.

5. Claims 36 and 41-43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Srinivasan.

Regarding claim 36, designating the most significant block identifier as most significant bits of a device index, and designating the most significant block index as least significant bits of the device index is not specifically disclosed in Srinivasan. However, in column 4, Lines 33-36, Srinivasan discloses generating an address for the most significant match. It would have been obvious to one skilled in the art at the time of the invention to construct the device index in the manner described in this claim. The motivation would be to indicate where the most significant match is located in the memory.

Regarding claim 41, determining the first MSSBPN and outputting first compare logic circuit control signal comprises: comparing the first SBPNS from the first and second DCBS to determine the MSSBPN; comparing the first MSSBPN with the first SBPN from the first DCB; generating a first control signal that indicates whether the first MSSBPN originates from the first DCB; comparing the first MSSBPN with the first SBPN from the second DCB; and generating a second control signal that indicates whether the first MSSBPN originates from the second DCB is not specifically disclosed in

Srinivasan. However, Srinivasan discloses in column 2, lines 41-47, a method that determines the highest priority piece of data in a memory and generates a control signal to indicate where it is, which is exactly what the described system does. It would have been obvious to one skilled in the art at the time of the invention to compare search words and generate control signals to indicate the highest priority data in a memory. The motivation would be to find the highest priority data in the memory.

Regarding claim 42, determining the second MSSBPN and outputting second compare logic circuit control signal comprises: assigning a LSSBPN to a second SBPN from the first DCB upon receiving the first control signal indicating that the first MSSBPN did not originate from the first DCB; assigning a LSSBPN to a second SBPN from the second DCB upon receiving the second control signal indicating that the first MSSBPN did not originate from the second DCB; comparing the second SBPNS from the first and second DCBS to determine the second MSSBPN; comparing the second MSSBPN with the second SBPN from the first DCB and generating a first output that indicates whether or not there was a match; and comparing the second MSSBPN with the second SBPN from the second DCB and generating a second output that indicates whether or not there was a match is not specifically disclosed in Srinivasan. However, Srinivasan discloses in column 2, lines 41-47, a method determines the highest priority piece of data in a memory and generates a control signal to indicate where it is, which is exactly what the described system does. It would have been obvious to one skilled in the ad at the time of the invention to compare search words and generate control signals to

indicate the highest priority data in a memory. The motivation would be to find the highest priority data in the memory.

Regarding claim 43, determining the second MSSBPN and outputting second compare logic circuit control signal further comprises: performing an OR function on the first control signal and the first output, and performing an OR function on the second control signal and the second output is not specifically disclosed in Srinivasan. However, the OR function is well known in the art. It would have been obvious to one skilled in the ad at the time of the invention to use an OR function. The motivation would be to use a well known function for which hardware is readily available.

***Conclusion***

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia L Davis whose telephone number is (571) 272-3117. The examiner can normally be reached on 8:30 to 6, Monday to Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu can be reached on (571) 272-3155. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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